Leakage Current Modeling of Series-Connected Thin Film Transistors

J. C. Sturm, I.-W. Wu, and M. Hack

Abstract—The leakage current of an arbitrary number of series-connected polysilicon Thin Film Transistors (TFT's) with a common gate is shown to be easily computed from the I-V characteristics of a single FET for the first time, both by an analytical model and by graphical techniques. Good agreement with experimental data is obtained for drain biases greater than ~1 V. The work is also applicable to single crystal Silicon-On-Insulator (SOI) TFT's.

I. INTRODUCTION

In many TFT applications, the leakage current of the TFT in the off state is a critical parameter for proper circuit operation. This may be driven by power concerns, as in SRAM technology [1], [2], or in Active Matrix Liquid Crystal Display (AMLCD's) technology, to improve the grey scale by stabilizing the voltage on the liquid crystal [3]–[5]. In AMLCD technology using polysilicon transistors, to reduce the leakage current it is common practice to replace a single transistor with multiple transistors in series connected to a common gate [4]. Because of the highly nonlinear device behavior of this regime, with two transistors in series leakage current reductions of over an order of magnitude are common.

The purpose of this letter is to show that the leakage current characteristics of such multiple TFT's in series can be quickly computed from the characteristics of a single FET, which has not been previously recognized. An analytical model is given which, based on two parameters of a single FET, predicts the leakage current reduction obtained by placing an arbitrary number of TFT's in series.

II. OVERVIEW AND GRAPHICAL ANALYSIS

When two transistors are connected in series (Fig. 1(a)) their drain currents must be equal, assuming no gate leakage. Therefore the voltage on the intermediate terminal, labeled $V_{D1}$, must adjust itself to this condition. When the gate voltage of a typical polysilicon NMOS TFT is below some nominal value, e.g., $-2 \text{ V}$ in Fig. 2, the leakage current rises as the gate-source voltage becomes more negative. This is due to high-electric field tunneling at specific trap sites near the high-field drain region [6]–[8], resulting in a channel current dominated by holes. Also, the leakage current in this regime increases strongly as the drain voltage is increased. The top transistor will have its source at a higher voltage than the lower one, and hence have a more negative $V_{GS}$ than the lower transistor. Therefore the applied $V_{DD}$ will divide itself so that most of the applied voltage falls across the lower transistor, giving it a larger $V_{DS}$ so that the two transistors have equal drain currents. When the gate voltage is such that the devices are in the classical subthreshold region and dominated by electron current in the channel ($V_{GS} > -2 \text{ V}$ in Fig. 1), $I_D$ increases exponentially with increasing $V_{GS}$ and is almost independent of $V_{DS}$, except decreasing with decreasing $V_{DS}$ for $V_{DS}$ much below 1 V. Because the lower transistor will have a more positive $V_{GS}$, causing a tendency toward much higher $I_D$, the drain voltage in this case will mostly fall on the upper transistor. Because of the the relatively weak $V_{DS}$ dependence in this case (versus the $V_{GS}$ dependence), a very small voltage is expected on $V_{D1}$ ($< 1 \text{ V}$) to accommodate for the difference in $V_{GS}$. These trends of voltage division were first qualitatively observed experimentally by Proano et al. [9] and then first analyzed (by performing a full 2-D two-carrier device simulation of the two transistor structure) in [10]. Because TFT's have no body effect, the I-V curves of Fig. 2 may be applied to either of the two FET's in series (with appropriate $V_{GS}$ and $V_{DS}$ definitions). Assuming the two FET's are independent

![Fig. 1. Schematic diagram of (a) two and (b) N TFT's in series to reduce leakage current.](image)

![Fig. 2. Measured I-V curves for a single polysilicon TFT ($W = 40 \mu m$, $L = 20 \mu m$). $V_{DS}$ varies from 0.1 to 10.1 V in 2.0 V steps. The gate oxide and channel polysilicon thicknesses were both 0.1 $\mu m$. No channel doping implant was performed. All process steps were at or below 600°C except a gate LTO oxygen densification step at 950°C (as in [7]).](image)
constructed solutions versus \( V_{GS} \). Note that for \( V_{GS} < -2 \) V, more than half of \( V_{DD} \) falls on the lower transistor, as expected. Why the fraction is a constant (~0.7) will be analytically shown in the next section. For \( V_{GS} > -2.0 \) V, \( V_{D,i} \) drops rapidly, with only ~0.5 V dropped on the lower FET for \( V_G = 0 \), consistent with the earlier discussion.

### III. Analytical Model

In this section, based on an approximation to the I-V characteristics of a single TFT for negative gate voltages, an analytical expression is derived for the leakage current reduction when \( N (N > 1) \) FET’s are connected in series compared to a single FET. Note that for sufficiently negative gate voltages, the drain current is exponentially dependent on both \( V_{GS} \) and \( V_{DS} \). For example, in Fig. 2 \( I_{DS} \) approximately triples when drain voltage is increased by 1 V (for \( V_{DS} > 1 \) V), and doubles when the gate voltage is decreased by 1 V. We may therefore approximate \( I_D \) as

\[
I_D = C e^{a V_{DS} - b V_{GS}}
\]  

(1)

where \( C \) is an arbitrary constant, and \( a \) and \( b \) are constants found from an individual TFT. \((a \approx \ln 3 \text{ V}^{-1} \text{ and } b \approx \ln 2 \text{ V}^{-1} \) for the data in Fig. 2). Although many groups have studied the physical mechanisms governing leakage current in TFT’s, (1) is not based on a physical model per se, but rather is based on an empirical fit to the data of Fig. 2. (Note (1) and the rest of the subsequent analysis is not valid for the low \( V_{DS} \) region (\( V_{GS} < 1 \) V) where the leakage current is dominated by electrons and is sublinearly dependent on \( V_{DS} \), and only applies for the high-field case (\( V_{DS} > 1 \) V). Using the notation of Fig. 1(b), expressing the \( V_{DS} \) and \( V_{GS} \) on each transistor in terms of \( V_{D,i} \), \( V_{G,i} \), applying (1), and equating the currents in transistors 1 and \( i-1 \), one finds the recursive relationship

\[
a V_{D,i} + (b - 2a) V_{D,i-1} + (a - b) V_{D,i-2} = 0,
\]

for \( i = 2 \) through \( N \).

Applying boundary conditions \( V_{D,N} = V_{DD} \) and \( V_{D,0} = 0 \), one can solve the above series of equations to yield

\[
\frac{V_{D,i}}{V_{D,1}} = \frac{a^i - (a - b)^i}{a^{i-1}b}.
\]

(3)

The fraction of the total drain voltage dropped over the lowest transistor (defined as \( \eta \)) is then

\[
\eta \equiv \frac{V_{D,i}}{V_{DD}} = \frac{a^{N-1}b}{a^N - (a - b)^N}.
\]

(4)

Since one now knows the drain voltage on the lowest transistor, one can easily calculate the leakage current for a given \( V_G \). Note that a fixed fraction of total drain voltage is dropped on the lowest transistor, independent of \( V_{GS} \). Because the leakage in the lowest transistor depends exponentially on the drain-source voltage, this implies a constant reduction in the drain current by a fixed factor independent of \( V_{GS} \). Therefore on a logarithmic scale, the I-V curves for negative \( V_{GS} \) of the multiply connected set have the same "shape" or slope as those of a single transistor. As mentioned earlier, this previously has been experimentally observed.
but its origin was not understood. The only previous analysis of this problem involved a first-principles, two-dimensional, two-carrier device simulation of a two-transistor structure which reproduced the experimental trend [10].

The leakage current of the N transistors \( I_{L,N} \) versus that of a single transistor \( I_{L,1} \) across \( V_{DD} \) is then

\[
\frac{I_{L,N}}{I_{L,1}} = e^{\frac{aV_{DD}}{2a-b}} = e^{-aV_{DD}/(2a-b)}. \tag{5}
\]

This is significant because it shows that the reduction in leakage current for multiple transistors in series can quickly be computed from the I-V curves of an isolated FET (without the need to derive a complicated device model that predicts the full range of I-V curves).

Note that in using (4) and (5), however, one must make sure that \( V_{GS} < -2 \) V (for the device of Fig. 2) and that \( V_{DS} > 1 \) V for all transistors because of the region of applicability of (1). In practice, this limits N to 3 for \( V_{DD} = 10 \) V and N to 4 for \( V_{DD} = 20 \) V. Note that because FET's in single crystal silicon have behavior for negative gate voltages qualitatively similar to that described by (1) [12], [13], this result should also be applicable to SOI TFT's (where the body effect is not significant).

In the common application case of \( N = 2 \), (4) and (5) reduce to

\[
\eta \equiv \frac{V_{DD,1}}{V_{DD}} = \frac{a}{2a-b} \tag{6}
\]

and

\[
\frac{I_{L,2}}{I_{L,1}} = e^{-a(a-b)V_{DD}/(2a-b)}. \tag{7}
\]

For the FET's of Fig. 2, from (5) one finds that \( \sim 0.7 \) of the applied \( V_{DD} \) will be dropped on the lower transistor. This is in good agreement with the graphical solution in Fig. 3 (\( \sim 7 \) V for \( V_{DD} = 10 \) V). For a \( V_{DD} = 10 \) V, (7) predicts a 19-fold decrease in leakage current. This is also in good agreement with the graphically constructed and experimental results, showing the usefulness of the analytical approach. (Note that our approach does ignore statistical variations from one FET to the next, however. This can be handled analytically, at least in the case of \( N = 2 \), by letting the three constants in (1) vary in each device. Such analysis will be addressed in future work.)

IV. SUMMARY

We have shown that the leakage current characteristics of multiple TFT's connected in series can quickly be computed from the characteristics of a single FET using an exponential model of the FET for for negative \( V_{GS} \). For negative gate voltages below the subthreshold region, the leakage current is reduced by a constant factor independent of \( V_{GS} \), and the largest fraction of the total drain voltage is dropped over the lowest FET. Once the subthreshold region is reached, however, most of the drain bias is dropped over the upper FET's.

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