p Channel thin film transistor and complementary metal–oxide–silicon inverter made of microcrystalline silicon directly deposited at 320°C

Y. Chen *, K. Pangal, J.C. Sturm, S. Wagner

Department of Electrical Engineering, Princeton University, Princeton, NJ 08544, USA

Abstract

We report a p channel thin film transistor (TFT) made of directly deposited microcrystalline silicon (μc-Si). The μc-Si channel material is grown by plasma-enhanced chemical vapor deposition (PECVD) using dc excitation of a mixture of SiH₄, SiF₄ and H₂, in a process similar to the deposition of hydrogenated amorphous silicon (a-Si:H). The deposition temperature for the μc-Si is 320°C and the highest post-deposition TFT process temperature is 280°C. By integrating this p TFT on a single μc-Si film with an n channel TFT, we fabricated a complementary metal–oxide–silicon (CMOS) inverter of deposited μc-Si. The p channel μc-Si TFT represents a breakthrough in low-temperature Si TFT technology because p channel TFTs of a-Si:H have not been available to date. The integrated CMOS inverter is the building block of a new digital circuit technology based on directly deposited μc-Si. © 2000 Elsevier Science B.V. All rights reserved.

1. Introduction

Considerable interest [1,2] exists in developing a large-area silicon technology produced at temperatures <350°C. This technology should be capable of furnishing the standard devices, including transistors, rectifying diodes and photodiodes, for applications in macroelectronics [1], and for add-on electronics to application specific integrated circuits (ASICs) [2]. ASIC applications require that all process temperatures be <400°C. In general, a reduction of the process temperature expands the applicability of macroelectronics. A usable ultra low-temperature (<350°C) technology needs p and n channels field-effect transistors, which are the building blocks for complementary digital circuits. Polycrystalline Si (poly-Si) TFTs are used for thin film complementary metal–oxide–silicon (CMOS) circuitry. However, the crystallization temperatures of 600°C employed for making polycrystalline silicon films motivate the search for a lower-temperature CMOS-capable Si TFT technology. n channel thin film transistors (TFTs) of hydrogenated amorphous silicon (a-Si:H), which can be made at temperatures of ~250°C, are widely used in large-area electronics [3]. However, no p channel TFTs have been made of a-Si:H because of the density of states in the lower half of its gap. Here we report the fabrication of a p channel TFT with a channel of directly deposited μc-Si. The resulting capability for CMOS circuits becomes a motive for developing TFTs with microcrystalline silicon (μc-Si) channels. Because...
direct deposition can be conducted at the relatively low temperature of plasma-enhanced chemical vapor deposition (PECVD) for a-Si:H [4,5], the low temperature of typically 300°C for direct deposition makes μc-Si accessible to a wider variety of substrates than those compatible with furnace and rapid thermal annealing [6]. Microcrystalline silicon also retains the advantages of a-Si:H such as film uniformity over large deposition areas.

n Channel TFTs made of directly deposited μc-Si have been reported earlier [7–11]. While μc-Si films can be obtained at temperatures as low as ~200°C [12], raising the growth temperature improves transistor performance, so that the μc-Si layers for these n channel TFTs typically were grown at higher temperatures, e.g., 350°C [8]. We fabricated the p channel thin film transistor from μc-Si deposited at 320°C, and processed the TFT at a maximum temperature of 280°C. We then integrated this p channel TFT with an n channel TFT to make the first μc-Si CMOS inverter. The μc-Si p channel TFT and integrated CMOS inverter are two key advances toward a complete, ultra low-temperature semiconductor technology based on directly deposited μc-Si.

2. Experiments

We describe the μc-Si CMOS process with Fig. 1. Substrates were unpassivated Corning 7059 glass. Both the p type and the n type TFTs use one single directly deposited μc-Si layer as the conducting channel. The μc-Si channel material is grown by PECVD in a process similar to the deposition of a-Si:H, using dc excitation of a mixture of SiH₄, SiF₄ and H₂. The undoped channel and the p⁺ and n⁺ contact layers were grown by PECVD in two separate (i layer, and doping) chambers. The SiO₂ gate dielectric also was grown by PECVD but in a separate system. Growth parameters are listed in Table 1. X-ray diffraction and Raman scattering [13], and an electron mobility of 4.9 cm²/V s in separately made n channel TFTs [10] prove that the films are microcrystalline. Adding SiF₄ to the source gas changes the growth chemistry [14], provides a wider range of structures [15], and a lower growth temperature [16] than

Table 1
Gas flow rates, deposition temperature, power density, pressure, and thickness of the films grown for the undoped μc-Si of the TFT channels, the doped source/drain contact layers, and the SiO₂ used for isolation

<table>
<thead>
<tr>
<th>Layers</th>
<th>SiH₄ (sccm)</th>
<th>H₂ (sccm)</th>
<th>SiF₄ (sccm)</th>
<th>PH₃, B₂H₆, or N₂O (sccm)</th>
<th>Temperature (°C)</th>
<th>Power density (mW/cm²)</th>
<th>Pressure (mTorr)</th>
<th>Film thickness (nm)</th>
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</thead>
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<tr>
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<td>20</td>
<td>0</td>
<td>320</td>
<td>160</td>
<td>900</td>
<td>300</td>
</tr>
<tr>
<td>p⁺ μc-Si</td>
<td>2</td>
<td>100</td>
<td>0</td>
<td>50</td>
<td>280</td>
<td>324</td>
<td>900</td>
<td>60</td>
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<tr>
<td>n⁺ μc-Si</td>
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<td>100</td>
<td>0</td>
<td>12</td>
<td>280</td>
<td>324</td>
<td>900</td>
<td>60</td>
</tr>
<tr>
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<td>0</td>
<td>0</td>
<td>160</td>
<td>250</td>
<td>85</td>
<td>400</td>
<td>200</td>
</tr>
</tbody>
</table>
deposition from H$_2$-diluted SiH$_4$ alone [15]. n channel TFTs of µc-Si grown with SiF$_4$ have the largest electron mobility reported to date [7]. The growth rate was 0.6 nm/s at a power density of 160 mW/cm$^2$. The dark conductivity of the i µc-Si is $1 \times 10^{-7}$ S/cm, and its thermal activation energy is 0.55 ± 0.05 eV. The p$^+$ and n$^+$ source/drain contact layers were grown from SiH$_4$, H$_2$ and B$_2$H$_6$ or PH$_3$ by RF excitation at 13.56 MHz. Their dark conductivities are 0.010 ± 0.001 S/cm (p$^+$ µc-Si) and 20 ± 2 S/cm (n$^+$ µc-Si).

The TFTs were made in the top-gate configuration shown in Fig. 1. The CMOS inverter is made of a p channel TFT and an n channel TFT of identical structure. A six-level mask process with masks designed in our laboratory were used in the inverter fabrication. The substrates were cleaned with the MICRO series 8790 glass-cleaning fluid (International Products Corporation) before deposition. First, 300 nm of i µc-Si and 60 nm of p$^+$ µc-Si layer were grown on the substrate without breaking vacuum. Next, we patterned the p$^+$ µc-Si source and drain for the p channel TFT using reactive ion etching (RIE) with 10% O$_2$ and 90% CCl$_2$F$_2$. The deposition of a layer of 200 nm isolation SiO$_2$ followed. Then we opened a window in the SiO$_2$ using buffered oxide etch (BOE) to deposit a 60 nm n$^+$ µc-Si layer. After RIE patterning of the n$^+$ µc-Si source and drain for the n channel TFT, we removed the SiO$_2$ layer with BOE, and followed by the definition of the i µc-Si island using RIE. The channel µc-Si now exposed was exposed for 10 min to 1:3 H$_2$O$_2$:H$_2$SO$_4$ for oxidation, then dipped for 10 s in BOE, rinsed in de-ionized water, blow-dried in nitrogen, and immediately introduced in the system for gate insulator deposition. After we deposited 200 nm SiO$_2$ as gate insulator, we patterned the SiO$_2$ gate and opened contact holes to the n and p channels TFT source and drain using BOE. Then we thermally evaporated Al, and patterned the Al using a wet-etch to form the gate, source and drain electrodes of the n and p channels TFTs, as well as the metal interconnects between the two gates, and the two drains of the p TFT and the n TFT. The pull-up p channel TFT and pull-down n channel TFT have 180 µm wide and 45 µm long channels. These large dimensions result from our use of a laser printer for mask making. The $\beta = (W_p/L_p)/(W_n/L_n)$ of the CMOS inverter, defined as the ratio of the width/length ratio of the pull-up p channel TFT over the width/length ratio of the pull-down n channel TFT, is 1. The TFTs and the inverters were measured with a HP 4155 parameter analyzer using its standard measuring program for FETs and inverters.

3. Results

Fig. 2 shows the transfer characteristics of the p channel TFT of the inverter. In the transfer characteristics the drain current, $I_d$, vs gate voltage, $V_{gs}$, was measured for drain voltages, $V_{ds}$, of −0.1 and −10 V. We define the ON current, $I_{ON}$, as the drain current, $I_d$, at a gate voltage, $V_{gs}$, of −25 V, and the OFF current, $I_{OFF}$, as the smallest drain current at a drain voltage of $V_{ds}$ of −10 V. Fig. 2 shows a p channel TFT ON/OFF current ratio of $>10^3$ when the gate voltage swings from −10 to −25 V, a threshold voltage, $V_{TH}$, of −16 V, and a subthreshold slope, $S = dV_{gs}/d \log_{10} I_d$, of 2.7 V/decade. The hole field-effect mobilities, $\mu_h$, of the p channel TFT extracted from the linear and saturated regimes are 0.023 and 0.031 cm$^2$/V s, respectively.

![Fig. 2. Transfer characteristics of the p channel µc-Si TFT of the CMOS inverter.](image-url)
Fig. 3 shows the transfer characteristics of the n channel µc-Si TFT of the CMOS inverter. The drain current, $I_d$, vs gate voltage, $V_{gs}$, was measured for drain voltages, $V_{ds}$, of 0.1 and 10 V. We define the ON current, $I_{ON}$, as the drain current, $I_d$, at a gate voltage, $V_{gs}$, of 25 V, and the OFF current, $I_{OFF}$, as the smallest drain current at a drain voltage of $V_{ds}$, of 10 V. The ON/OFF current ratio of the n channel TFT of Fig. 3 is $10^4$, its $V_{TH}$ is 3 V, and $S = 4.2$ V/decade. The electron field-effect mobilities, $\mu_n$, of the n channel TFT extracted from the linear and saturated regimes are 0.72 and 1.0 cm$^2$/V s, respectively.

The voltage transfer characteristic of the first µc-Si CMOS inverter made of the pull-up p channel TFT and the pull-down n channel TFT is shown in Fig. 4 for supply voltages of $V_{DD} = 30$ V and $V_{SS} = -20$ V. The inverter has a nearly full rail-to-rail swing, and a well-defined voltage transfer characteristic with a gain of 7.2, measured from the slope of the voltage transfer curve in the transition region. The output HIGH is about 90% of the full voltage range and the output LOW is at the same voltage as $V_{SS}$.

4. Discussion

The linear and saturated hole mobilities in the p channel TFT are 0.023 and 0.031 cm$^2$/V s, respectively. While these values are small compared to those of n channel TFTs, they do demonstrate p channel operation. The threshold voltage of $-16$ V indicates that the channel film may be slightly n type, so that it needs extra gate voltage to invert the conducting channel. For a threshold voltage shift of $-10$ V of the TFT compared to the TFT with a channel free of n type dopant, we deduce an effective interior n type dopant density of $1 \times 10^{17}$ cm$^{-3}$, using the following formula [17]:

$$V_{TH} = V_{FB} - 2\phi_p - (4\varepsilon_0 q N_d \phi_p)^{1/2} / \varepsilon_{ox},$$

(1)

where $V_{FB}$ is the flat band voltage, $\phi_p$ the bulk potential, $\varepsilon_0$ the dielectric constant of silicon, $q$ the electronic charge, $N_d$ the effective n type dopant density and $\varepsilon_{ox}$ is the gate capacitance per unit area.

For the n channel TFT the linear and saturated $\mu_n$ of 0.72 and 1.0 cm$^2$/V s, respectively, are less than those obtained in a separately fabricated µc-Si n channel TFT [11]. We ascribe the reduction in field-effect mobility to the unoptimized process sequence for CMOS inverter fabrication, which also is observed in $V_{TH}$ and $S$. The CMOS inverter has an almost full rail-to-rail output voltage swing and a transition. The output HIGH does not reach $V_{DD}$ because of the smaller ON current of the p channel TFT, and the larger leakage current of the n channel TFT.
at larger negative gate bias. The larger leakage current can be explained by thermionic field emission of carriers through the grain boundary trap states [18]. The µc-Si TFTs need improvements in two directions. One is larger field-effect mobilities, to enable larger ON current for greater speed and fan-outs. The other is a further reduction in process temperature, to take advantage of a wider variety of substrate materials. The inverter must be redesigned with a larger β to optimize its performance.

5. Conclusion

We report the first p channel TFT made of directly deposited µc-Si. The µc-Si channel material is grown by PECVD at 320°C and the highest post-deposition TFT process temperature is 280°C. By integrating this p TFT with its n channel counterpart on a single µc-Si film, we fabricated the first CMOS inverter of deposited µc-Si. The low-temperature p channel µc-Si TFT and the integrated CMOS inverter represent a digital device and circuit technology based on directly deposited microcrystalline thin film silicon. Its maximum process temperature of 320°C is ideally suited to glass substrates. It also is suited as a CMOS technology for add-on circuits to ASICs.

References