transport, then air-annealed at different temperatures transform the bound excition emission. Specifically, the IΓ intensity decreases significantly as annealing temperature increases. Conversely, this IΓ emission increases dramatically with hydrogenation, regaining almost all the intensity lost due to annealing. To detect Hall variations, given the small - tens of nanometers - SIMS-measured penetration depth of the H- plasma ions, we employed two approaches: (1) reducing the initial bulk carrier concentration by compensating via Li in-diffusion, (2) using an epitaxial thin film of ZnO on sapphire to minimize the thickness of the conductive layer relative to the diffusion depth of hydrogen species. Li doping removed the IΓ line and subsequent hydrogenation reintroduced broader emission in the IΓ region. Li doping removed the initial ~1017 cm-3 carrier concentration whereas hydrogenation restored detection of the conductivity and Hall coefficient. For a hydrogenated thin film grown on sapphire by molecular beam epitaxy, we observed an order of magnitude increase in the spectral profile confirms that the carrier concentration has been graded as expected. The expected current-voltage characteristics have been measured. The idea factor extracted from the J-V curve in the forward direction is about 1.78, and reverse saturation current is very low, about 0.2nA/cm2. The spectral response on the AlGaAs drift cell shows 40-45% internal quantum efficiency at green and orange and 20-35% at longer wavelengths. However, the response at blue-UV range is very low, which we currently think is due to the carriers generated by UV-blue photon absorption recombining via interstitial Be traps in the heavily p-doped (1018 cm-3) region near the AlGaAs surface. Details of the high-energy photon loss mechanism will be presented at the conference.

3:10 PM Break

Session J: Si-Based Heterojunctions and Strained Si: Growth, Characterization and Applications

Wednesday PM Room: 141
June 23, 2004 Location: DeBartolo Hall

Session Chairs: Sarah H. Olsen, University of Newcastle-upon-Tyne, Newcastle NE1 7RU UK; Doug Webb, ATMI, Meza, AZ 85210 USA

3:30 PM J1. High Electron Mobility Transistor Structures on Sapphire Substrates Using CMOS Compatible Processing Techniques: Carl H. Mueller; Samuel A. Alterovitz; Edward T. Croke; George E. Ponchak; 1Analex Corporation, 21000 Brookpark Rd., MS 7-1, Brookpark, OH 44135 USA; 2NASA Glenn Research Center, 21000 Brookpark Rd., MS 54-5, Cleveland, OH 44135 USA; 3HRL Laboratories, 3011 Malibu Canyon Rd., RL63, Malibu, CA 90265 USA; 4NASA Glenn Research Center, 21000 Brookpark Rd., MS 54-5, Cleveland, OH 44135 USA

System-on-a-chip (SOC) processes are under intense development for high-speed, high frequency monolithic circuits. As frequencies, data rates, and circuit complexity increases, the need for substrates that enable high-speed analog operation, low-power digital circuitry, and excellent isolation between devices becomes increasingly critical. SiGe/ Si modulation doped field effect transistors (MODFETs) with high carrier mobilities are currently under development to meet the active RF device needs. However, as the substrate normally used is Si, the low-to-modest substrate resistivity causes large losses in the passive elements required for a complete high frequency circuits. These losses are projected to become increasingly troublesome as device frequencies progress to the Ku-band (12 - 18 GHz) and beyond. Relative to Si, the high electrical resistivity of sapphire enables superior performance in passive device such as inductors, and less cross-talk between devices. Sapphire is an excellent substrate for high frequency SOC designs because it supports excellent both active and passive RF device performance, as well as...
low-power digital operations. We are developing high electron mobility SiGe/Si transistor structures on r-plane sapphire, using either in-situ grown n-MODFET structures or ion-implanted high electron mobility transistor (HEMT) structures. Advantages of the MODFET structures include high electron mobilities at all temperatures (relative to ion-implanted HEMT structures), with mobility continuously improving to cryogenic temperatures. We have measured electron mobilities over 1,200 and 13,000 cm²/V·sec at room temperature and 0.25 K, respectively, in MODFET structures. The electron carrier densities were 1.6 and 1.3x10¹² cm⁻² at room and liquid helium temperature, respectively, denoting excellent carrier confinement. Shubnikov-de Haas oscillations were observed, thus confirming the 2D nature of the carriers. Conversely, HEMT structures using ion-implanted processing are appealing because they are compatible with existing CMOS processing, and thus would be attractive for complex, highly integrated circuitry. Using this technique, we have observed electron mobilities as high as 900 cm²/V·sec at room temperature, at a carrier density of 1.3x10¹² cm⁻². The temperature dependence of mobility for both the MODFET and HEMT structures provides insights into the mechanisms that allow for enhanced electron mobility as well as the processes that limit mobility, and will be presented. Using the MBE Sb doped structures, transistors with varying source-to-drain distances and gate lengths (1 - 5 µm) were fabricated. Although the design is not optimized, the initial results are promising. The I-V behavior indicated the saturated drain current region extended over a wide drain voltage range, with knee voltages of approximately 0.5 V and increased leakage starting at voltages slightly higher than 4 V. The saturation drain currents were lower than expected, and reasons for this are under investigation.

3:50 PM Student  
J2, Temperature Sensitivity of DC Operation of Sub-Micron Strained Si MOSFETs: Valerio Gaspari1; Kristel Fobelets2; Sarah H. Olsen2; Jesus Enrique Velazquez-Perez2; Anthony G. O’Neill3; Jing Zhang1; 1Imperial College London, Elect. & Elect. Engrg., MailStop EEE-OSD, Exhibition Rd., London, England SW7 2BT UK; 2University of Newcastle upon Tyne, Elect. Engrg., Newcastle NE1 7RU UK; 3Universidad de Salamanca, Dept. de Física Aplicada, Edificio Trilingüe, P.za de la Merced s/n, Salamanca E-37008 Spain; 4Imperial College London, Physics, Exhibition Rd., London SW7 2AZ UK. 

The DC performance of sub-micrometer Strained-Si n-type surface channel MOSFETs has been investigated for operating temperatures ranging from 10 K to 300 K. The strained-Si layer that constitutes the active region of the devices was grown on strain-relaxed constant-composition SiGe buffer layer, preceded by a linearly graded SiGe virtual substrate. The low-field maximum transconductance of MODFET and HEMT structures provides insights into the mechanisms that allow for enhanced electron mobility as well as the processes that limit mobility, and will be presented. Using the MBE Sb doped structures, transistors with varying source-to-drain distances and gate lengths (1 - 5 µm) were fabricated. Although the design is not optimized, the initial results are promising. The I-V behavior indicated the saturated drain current region extended over a wide drain voltage range, with knee voltages of approximately 0.5 V and increased leakage starting at voltages slightly higher than 4 V. The saturation drain currents were lower than expected, and reasons for this are under investigation.

4:30 PM Student  
J4, Uniaxially-Tensile Strained Ultra-Thin Silicon-On-Insulator with Up to 1.0% Strain: R. L. Peterson1; H. Yin2; K. D. Hobart3; T. S. Duffy4; J. C. Sturm5; 1Princeton University, Dept. of Elect. Engrg., E-Quad, Olden St., Princeton, NJ 08544 USA; 2Naval Research Laboratory, Washington, DC 20375 USA; 3Princeton University, Dept. of Geosci., Guyot Hall, Princeton, NJ 08544 USA.

Low uniaxial tensile strain of <0.04% has been recently reported to increase both PMOS and NMOS silicon-on-insulator (SOI) effective mobilities by ~15%, much more than that expected by comparable biaxial strain.1 We have demonstrated uniaxial tensile strain in SOI of 0.6% using stress balance of a SiGe/Si bi-layer structure.1 In this study, record uniaxial strain of 1.0% has been achieved by thinning the Si film in the bi-layer. This increased strain level should allow for greater device performance enhancement. SiGe and Si films are transferred to a BPSG (borophosphorosilicate glass)-coated Si wafer by a wafer bonding process and are 3 orders of magnitude lower than those reported for HfO₂ on Ge for similar EOTs. We attribute this leakage reduction to the epitaxial Ge layer and high-k dielectric layer being grown without breaking the vacuum, thus avoiding interfacial contamination. Thus, low temperature MOS capacitor stacks with strained epitaxial Ge or Si₁₋ₓGex layers directly on Si substrates, and with HfO₂ (EOT=9.7 Å) as dielectric, both using RPCVD is demonstrated. Well behaved MOS capacitors show that RPCVD process is a promising technique for low thermal budget, high performance applications.
quickly expand in the short dimension (≤ 20µm), yielding uniaxial tensile Si strain. The net strain change is identical for the Si and SiGe films because of their coherent interface. That the two layers move together is clearly demonstrated for 20µmx150µm islands of 30nm SiGe/25nm Si/200nm BPSG, before and after 30min at 800°C in nitrogen: \( \Delta \varepsilon_{SiGe} = \Delta \varepsilon_{Si} = 0.75\% \). To obtain larger uniaxial Si strain we use a thinner layer of Si: 30nm SiGe/10nm Si/5.5nm SiN, / 1µm BPSG. SiN\(_{x}\) is added to suppress dopant out-diffusion from BPSG. After 15min at 750°C, SiGe strain in the short-dimension direction changes from 1.2% to 0.2% (i.e., from full compressive strain to almost complete relaxation) in agreement with predicted SiGe strain of 0.2% based on stress balance. The resulting uniaxial tensile strain in the underlying 10nm Si layer is directly measured to be 1.0%, again confirming a coherent SiGe/Si interface. For stress balance of the same bi-layer, uniaxial Si strain is greater than biaxial Si strain (~0.7%) due to the long island dimension constraint, which is important for SiGe thickness to take place in the short dimension. 1B.M. Haugerud, et. al., Journal of Applied Physics, 94, 4110 (2003) 2S. Takagi, et. al.,IEDM Digest, Washington, DC (2003), pp.57-60 H. Yin, et. al., MRS Fall Meeting, Boston, MA (2003) 3H. Yin, et. al., Journal of Applied Physics, 91, 9716 (2002) 4H. Yin, et. al., IEDM Digest, Washington, DC (2003) 5S.C. Jain, et. al., Physical Review B, 52, 6247 (1995).

4:50 PM  

Student: J5, Influence of the Si-Ge Interdiffusion in NiSi\(_{1-x}\)Ge\(_x\) on Morphological Stability: Johan Seger\(^1\); Tobias Jarma\(^2\); Fredric Ericson\(^2\); Ulf Smith\(^2\); Shi-Li Zhang\(^3\); 1KTH, Dept. of Microelett. & Info. Tech., PO Box E229, Kista SE-164 40 Sweden; 2Uppsala University, The Ångström Lab., Matl. Sci., PO Box 534, Uppsala SE-751 21 Sweden

In order to meet the requirements specified in the International Technology Roadmap for Semiconductors (ITRS), for realization of the aggressive downscaling, new materials need to be introduced. The regions of interest here are the source/drain (S/D) where shallow junctions need to be combined with low sheet resistance and low resistivity contacts, and the channel where high mobility is essential for high performance nano-MOSFETs. This so-called “material scaling” leads to a requirement for the integration of new materials in standard Si processing technology. One of the most promising candidates for the “material scaling” approach is Si\(_{1-x}\)Ge. The incorporation of compressively strained Si\(_x\)Ge in a MOSFET, i.e. in the channel region or in S/D, has made the study of phase and morphology stabilities in NiSi\(_{1-x}\)Ge\(_x\) on Si\(_{1-x}\)Ge\(_x\) particularly interesting. The poor morphological stability of NiSi\(_{1-x}\)Ge\(_x\), formed on Si, ,Ge\(_x\) is of a serious concern when forming contacts based on self-aligned silicid (silicide) technology. Our recent studies show that the agglomeration of NiSi\(_{1-x}\)Ge\(_x\) begins already around 550 °C and is independent of the crystallinity of the underlying Si\(_{1-x}\)Ge\(_x\) film, polycrystalline or single-crystal. We have identified that interdiffusion of Si and Ge inside the germanosilicide grains is a major cause for agglomeration. In the present work, we study the Si-Ge interdiffusion in NiSi\(_{1-x}\)Ge\(_x\) using various single-crystal Si\(_{1-x}\)Ge\(_x\) films of different compositions and different thickness combinations.Compressively-strained Si\(_x\)Ge layers were grown epitaxially on Si(100) with chemical vapor deposition. Nickel films were deposited by means of electron-beam evaporation. The samples were annealed rapidly thermally. A four-point probe was used to measure the sheet resistance in order to monitor the solid-state interaction as well as to correlate the resistance variation to the evolution of the surface morphology. Phase identification was carried out using X-ray diffraction. Scanning transmission electron microscopy in combination with energy dispersive spectroscopy was used to detail the morphology of the interface region. Our results show that a substantial interdiffusion of Si and Ge inside the NiSi\(_{1-x}\)Ge\(_x\) grains already occurs at 600 °C. The atomic movement of the least mobile species at such low temperatures results in a rapid composition homogenization of a NiSi\(_{1-x}\)Ge\(_x\)/NiSi bilayer structure and a hindrance of the undesired NiSi\(_x\)formation. It also leads to an improved morphological stability of the NiSi\(_{3/4}\)Ge\(_{1/4}\)/NiSi structure on Si, compared to the stability of NiSi\(_{1/2}\)Ge\(_{1/2}\) on Si\(_{3/4}\)Ge\(_{1/2}\). Our investigation also shows that the film texture of NiSi\(_{1-x}\)Ge\(_x\) is strongly affected by the characteristics of the Si\(_{1-x}\)Ge\(_x\) layer and it is found that the layer sequence of the various Si\(_{1-x}\)Ge\(_x\) layers influences the film texture. Ni interaction with the Si\(_{3/4}\)Ge\(_{1/2}\)Si structure leads to a preferentially orien-
ted textured NiSi\(_{1-x}\)Ge\(_x\) film whereas NiSi\(_{1-x}\)Ge\(_x\) formed on the Si/Si\(_{3/4}\)Ge\(_{1/2}\) system gives a randomly orientated silicide film.

### Session K: Quantum Dots in III-V and Group IV Compounds

**Wednesday PM**  
**Room**: 136  
**Location**: DeBartolo Hall

**Session Chair**: Ben Shanabrook, Naval Research Laboratories, Nanostructures Section, Washington, DC 20375-5000 USA

**1:30 PM**

**K1, Thermal Processing of InAs and InGaAs Quantum Dots for Device Integration**: Forrest Klaat\(^1\); Jeff Cederberg\(^2\); 1Sandia National Laboratories, PO Box 5800, Albuquerque, NM 87185 USA

Semiconductor quantum dots are being investigated to take advantage of the effects of three-dimensional quantum confinement for optoelectronic devices. We are investigating InAs and InGaAs quantum dots formed by metal-organic chemical vapor deposition. The incorporation of quantum dots into integrated devices requires evaluation of their optical properties after thermal treatments used to modify the ground state energy. The InAs quantum dots investigated have a ground state at 1130 meV (1100 nm) when grown directly on GaAs layers. Investigations looked at a matrix of thermal treatments ranging from 600 to 900 C and times from 15 seconds to 1 hour. For samples annealed in contact with a GaAs wafer (proximity capping), we have observed a blue shift in the peak energy of 40 meV at 600°C for treatment times of 10 minutes. Extending this treatment out to 1 hour produces a 112 meV shift in the ground state. The emission intensity is retained for temperatures up to 650 C for the times investigated, but higher temperatures result in significant intensity degradation, possibly due to non-radiative recombination at point defects formed during treatment. Quantum dot emission is not observed when the sample is annealed at 900 C for any length of time, setting a maximum processing temperature. Samples capped with PECVD SiO2 and annealed have similar annealing characteristics, however, the magnitude of the blue shift is reduced compared to the proximity capped samples. The origin of this effect is not clear, since SiO2 capping is known to enhance the disordering of quantum well structures.

In0.40Ga0.60As quantum dots emitting at 1050 nm, treated using similar conditions, will be compared to the InAs structures to evaluate their thermal stability. Our results will be contrasted with results from the literature. Support from the Division of Materials Science and Engineering, Office of Science, U.S. Department of Energy, is gratefully acknowledged.

**1:50 PM**

**K2, Thermal Effect on the Luminescence Properties of InP Quantum Dots Coupled with an InGaP Quantum Well Through a Thin InAlGaP Barrier**: X. B. Zhang\(^1\); J. H. Ryoo\(^2\); G. Walter\(^2\); N. Holonyak\(^2\); R. D. Dupuis\(^3\); 1Georgia Institute of Technology, Sch. of Electric & Computer Engr., Atlanta, GA 30332 USA; 2University of Illinois, Micro & Nanotech Lab., Urbana, IL 61801 USA

InP self-assembled quantum dots (SAQDs) or simply QDs) on InGaP matrices have been studied by several research groups and on InGaAlP and InAlP matrices by the present authors. Lasers emitting in the red spectral region operating CW at 300K were realized by using In0.5(A10.6Ga0.4)0.5P as the confining layer. We have demonstrated that by using an auxiliary InGaP quantum well (QW) coupled to InP QDs through a thin InAlGaP barrier layer (QW+QD structure), the carrier collection efficiency and the operation of QD lasers can be markedly improved. The QW with a thin barrier used here not only helps the thermalization of injected hot carriers in QW before they tunnel into the QDs but also helps the carrier injection in QDs. Furthermore, the thin barrier between the QW and QD layers can be used to adjust the uniformity and the density of QDs. This improved laser operation was also realized in the InAs QW+QD system. On the other hand, by directly